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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/681,414 | 10/08/2003 | Ebrahim Abedifard | 400.241US01 | 7409 |

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| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/681,414 | ABEDIFARD, EBRAHIM |
| | Examiner | Art Unit |
| | Thong Q. Le | 2827 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-11 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18 and 19* is/are allowed.

6)☒ Claim(s) *9,13,16,17,20 and 22* is/are rejected.

7)☒ Claim(s) *10,11,14,15 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION.

1. Amendment filed on 07/13/2005 has been entered.

2. Claims 9-11,13-22 are presented for examination.

### *Response to Arguments*

3. Applicant's arguments with respect to claims 9-11,13-22 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 9, 13, 16-17, 20, 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanzawa et al. (U.S. Patent No. 6,605,986).

Regarding claim 9, Tanzawa et al. disclose a flash memory device (Figure 1) comprising:

a plurality of n-wells (Figure 1, 72) comprising an n-type conductivity material formed in a p-type substrate (Figure 1, 71) ;

a plurality of p-wells (Figure 1, 73) comprising a p-type conductivity material, each p-well located within an n-well;

a plurality of flash memory array blocks (Figure 2) , each comprising a plurality of flash memory cells arranged in rows (Figure 2) that are coupled together by wordlines (Figure 2, WL), each flash memory array block located within a different p-well of the plurality of p-wells (Figure 2) ; and

a row decoder (Figure 16, 49) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.

Regarding claims 13, 16-17, Tanzawa et al. disclose a flash memory device (Figure 1) comprising:

a plurality of lower wells comprising a first conductivity material (Figure 1, 72) formed in a substrate (71) comprising a second conductivity material;

a plurality of isolation wells (73) comprising the second conductivity material, each isolation well located within a lower well;

a plurality of flash memory array blocks (Figure 2) , each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines (Figure 2,

WL), each flash memory array block located within a different isolation well of the plurality of isolation wells (Figure 2) ; and

a row decoder (Figure 16, 49) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.

Regarding claim 20, Tanzawa et al. disclose for erasing a memory cell in a memory array block of a plurality of memory array blocks, each memory array block located within a first conductivity material that is located within a second conductivity material, the method comprising: generating an address signal of the memory cell; a row decoder selecting, in response to the address signal, a wordline signal that is coupled to the memory cell, the wordline signal additionally coupled to the plurality of memory array blocks; and coupling a voltage that is less than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal (Column 19, TABLE 3 , (-1), Erase verify, Non-selected WORD LINE).

Regarding claim 22, Tanzawa et al. disclose an electronic system (Figure 16) comprising:

a processor (48) that controls operation of the electronic system and generates address signals and

a flash memory device (Figure 16) coupled to the processor, the device comprising:

a plurality of lower wells comprising a first conductivity material (Figure 1, 72) formed in a substrate (71) comprising a second conductivity material;

a plurality of isolation wells (73) comprising the second conductivity material, each isolation well located within a lower well;

a plurality of flash memory array blocks (Figure 2) , each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines (Figure 2, WL), each flash memory array block located within a different isolation well of the plurality of isolation wells (Figure 2) ; and

a row decoder (Figure 16, 49) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.

6. Claims 9, 13, 16-17, 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano (U.S. Patent No. 6,747,901).

Regarding claim 9, Hirano discloses a flash memory device (Figure 2) comprising:

a plurality of n-wells (Figure 2, 11) comprising an n-type conductivity material formed in a p-type substrate (Figure 2, 10, ABSTRACT, Column 6, lines 11-13) ;

a plurality of p-wells (Figure 2, 12) comprising a p-type conductivity material, each p-well located within an n-well;

a plurality of flash memory array blocks (Figure 1) , each comprising a plurality of flash memory cells arranged in rows (Figure 1) that are coupled together by wordlines (Figure 1, WL), each flash memory array block located within a different p-well of the plurality of p-wells (Figure 1) ; and

a row decoder (Figure 1, RD) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.

Regarding claims 13, 16-17, Hirano discloses a flash memory device (Figure 1) comprising:

a plurality of lower wells comprising a first conductivity material (Figure 2,11) formed in a substrate (Figure 2, 10) comprising a second conductivity material;

a plurality of isolation wells (Figure 2, 12) comprising the second conductivity material, each isolation well located within a lower well;

a plurality of flash memory array blocks (Figure 1) , each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines (Figure 1, WL), each flash memory array block located within a different isolation well of the plurality of isolation wells (Figure 1) ; and

a row decoder (Figure 1, RD) coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.

***Allowable Subject Matter***

7. Claims 10-11,14-15, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-11,14-15, 21 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Tanzawa et al. (U.S. Patent No. 6,605,986), Hirano (U.S. Patent No. 6,747,901), and others, does not teach the claimed invention having wherein a voltage of 0V is applied to the n- well and a voltage of -5V is applied to the p-well of an unselected flash memory array block during an erase operation, and wherein a voltage of 5V is applied to the n- well and a voltage of 5V is applied to the p-well of an unselected flash memory array block during a program operation.

8. Claims 18-19 are allowed.

Claims 18-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Tanzawa et al. (U.S. Patent No. 6,605,986), Hirano (U.S. Patent No. 6,747,901), and others, does not teach the claimed invention having a first voltage that is greater than 0V to the first conductivity material of memory array blocks that are not selected by the wordline signal, and a second voltage that is greater than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER